SCIENCE
PASSION
TECHNOLOGY

Aloha-HE

A Low-Area Hardware Accelerator for Client-Side Operations in Homomorphic Encryption

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January 31, 2024

Outline

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Homomorphic Encryption (in short HE)

- Special encryption technique
- Computations directly on encrypted data
  - Confidential cloud computing
  - Sensitive data processing on untrusted third parties
  - Novel opportunities

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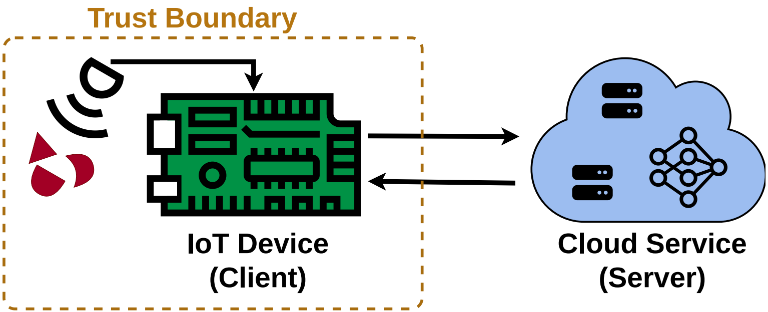

- Encrypts sensitive data
- Sends it to cloud

- Computes on encrypted data
  - E.g.: AI application
- Returns result to client

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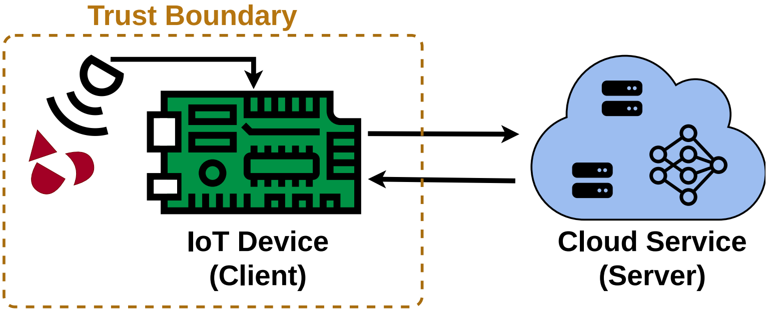

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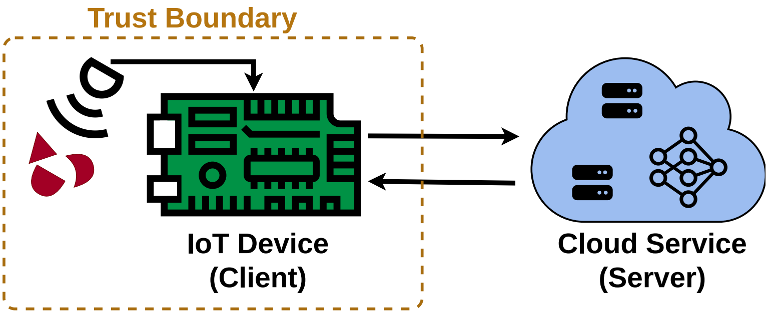

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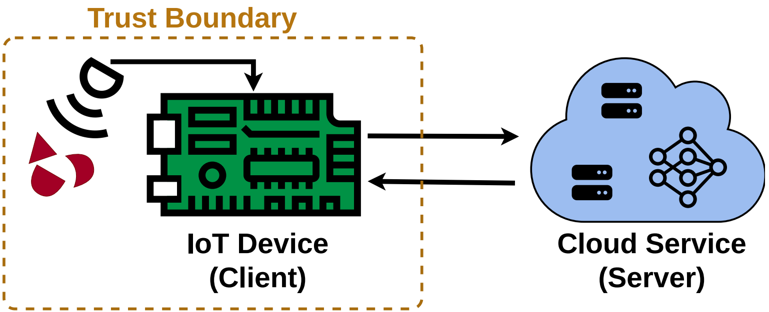

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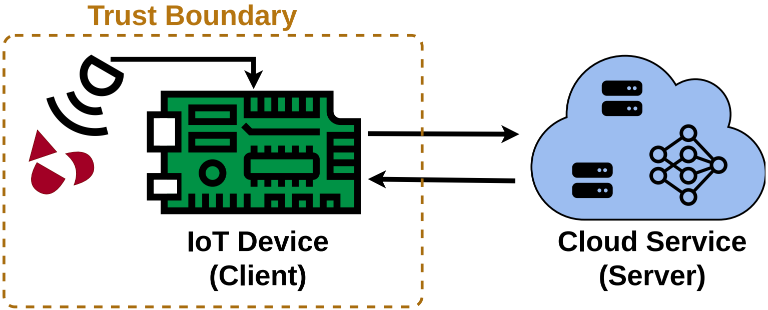

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Hardware acceleration!

State of the art in accelerating HE

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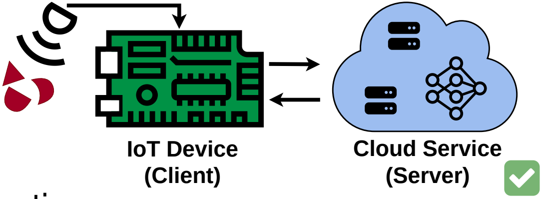

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  - Usually the limiting factor
- **But:** Client-side is also crucial in constrained scenarios

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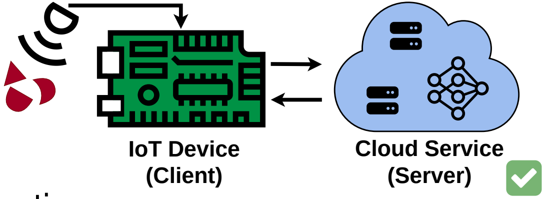

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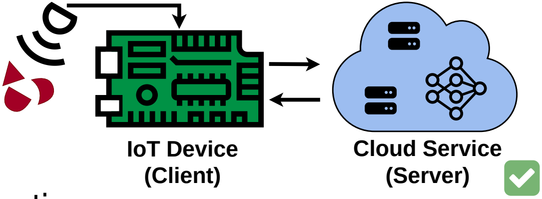

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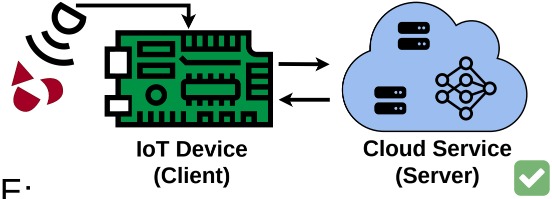

- Consider IoT application with HE:
  - Timely tasks require fast encryption/decryption
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  - Low-cost devices
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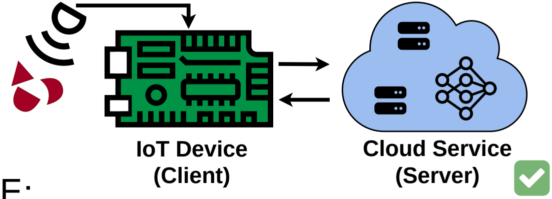

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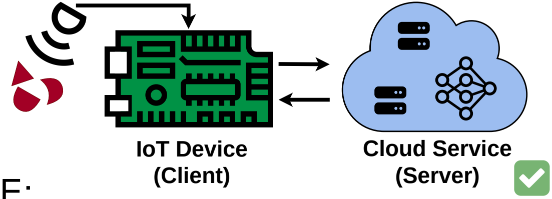

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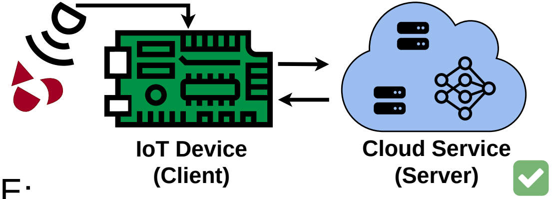

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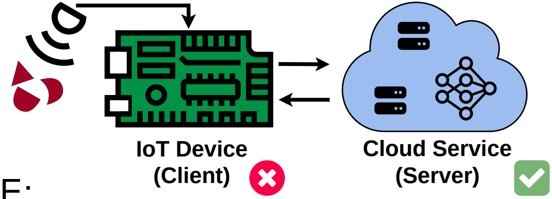

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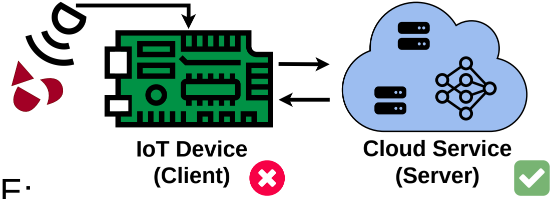

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} Motivation for Aloha-HE

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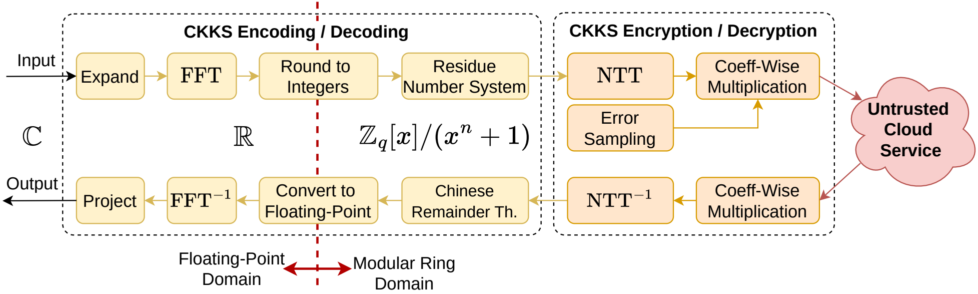

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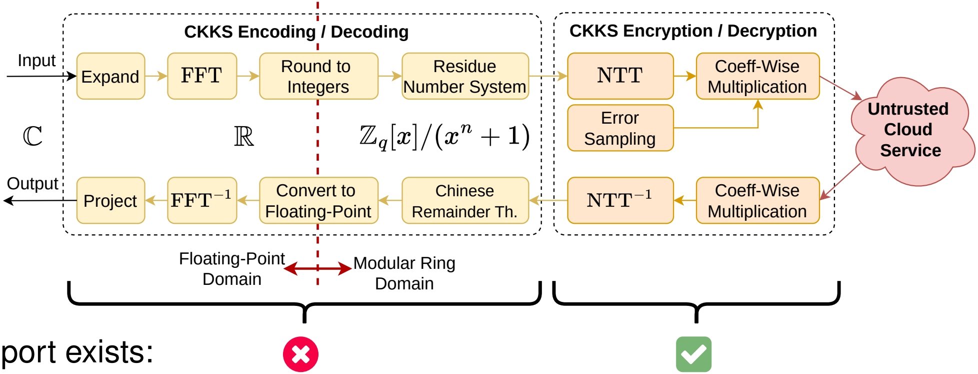

HW support exists:

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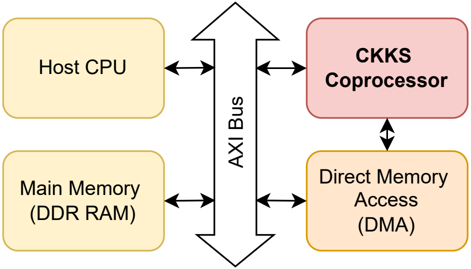
Overall Architecture



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- DMA for data streaming
- CPU controls DMA and coprocessor
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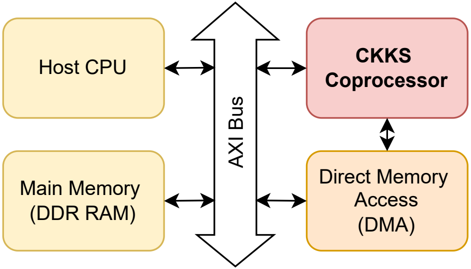

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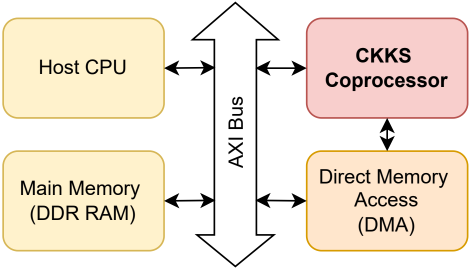

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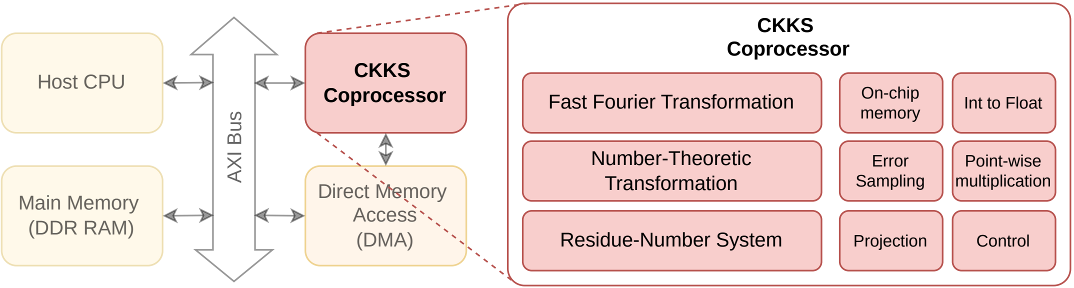
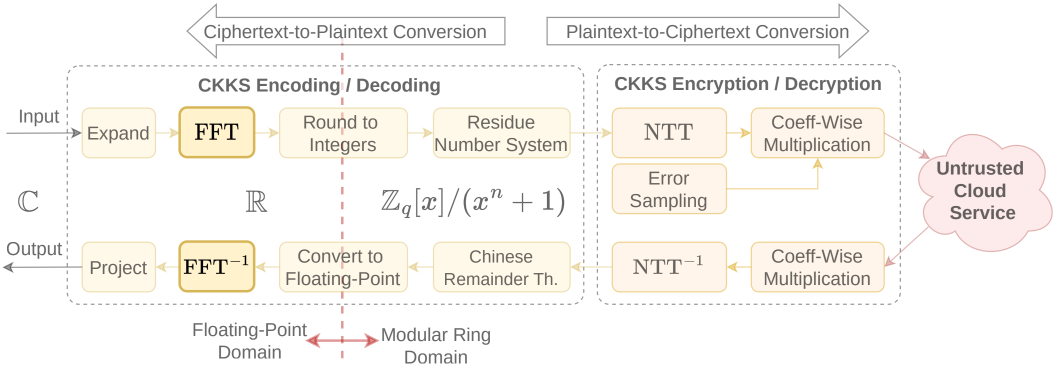
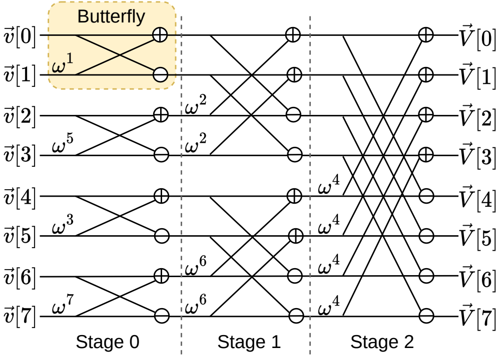


Fast Fourier Transformation



Fast Fourier Transformation: Data Flow

- Basic operation: Butterfly
- Iterated within $\log_2(n)$ stages
- Requires twiddle factors ω^i
  - Roots of unity in $\mathbb{C}$



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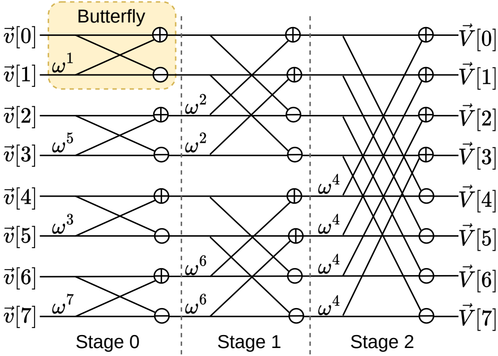

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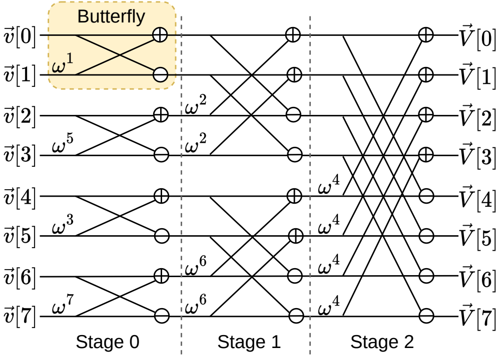

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  - Needs to support complex addition and multiplication
  - Must fit on small area
  - Optimized for FFT computation

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- Sharing of resources within the FFT butterfly
  - ➔ lowering area consumption
- Stored *or* on-the-fly generated twiddle factors
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- Reducing the number of stored twiddle factors by 75%
  - ➔ lowering BRAM consumption

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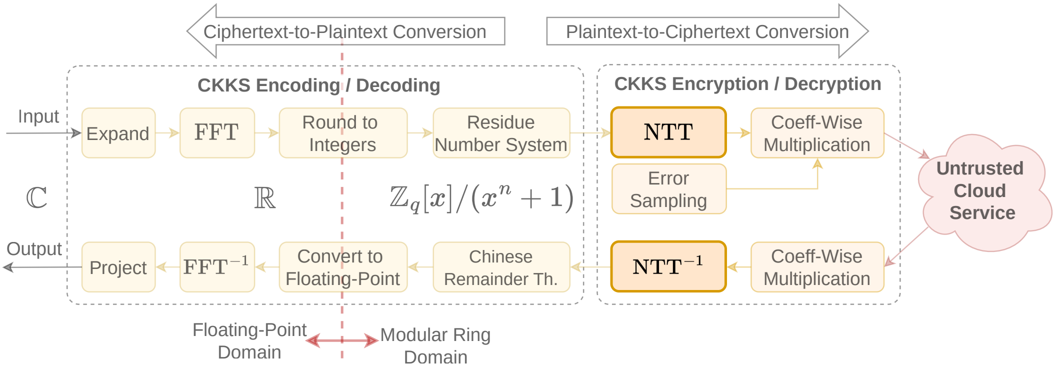

Number-Theoretic Transformation

- Operates over modular ring domain $\mathbb{Z}_q$
  - Ring arithmetic modulo prime q
- Special properties of NTT:
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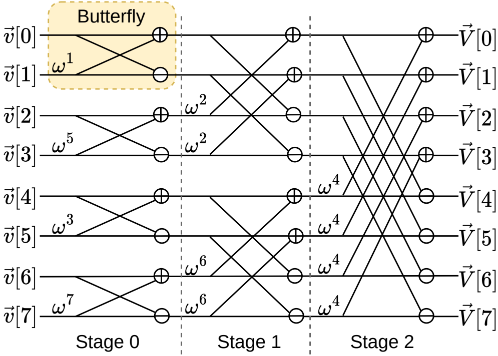
- Execution flow of NTT is identical to FFT
  - Share control logic
  - Share load and store logic
- Just underlying arithmetic is different
  - But still allows resource sharing!



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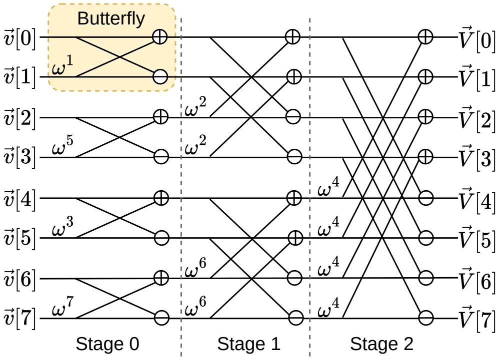

Sharing of Integer Multipliers

- FFT instantiates four floating-point multipliers

$$(a_r + \mathrm{i}a_i)(b_r + \mathrm{i}b_i) = (a_r b_r - a_i b_i) + \mathrm{i}(a_r b_i + a_i b_r)$$

➔ each contains one integer multiplier

Use the existing integer multipliers in NTT!

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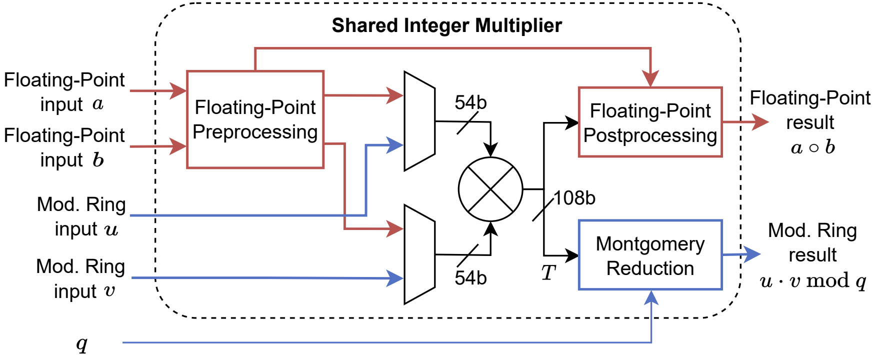

Sharing of Integer Multipliers: Benefits

- 1 complex multiplier $\leftrightarrow$ 4 modular ring multipliers
- Reused for 3 concurrent NTT + 1 twiddle factor generation
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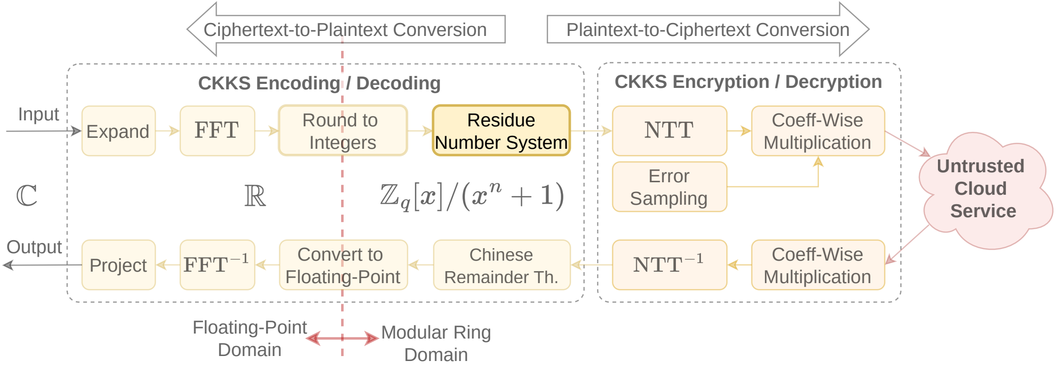

Residue Number System (in short RNS)

- Reduces computational complexity
- Splits large encoded value x into multiple smaller values $(x_0, \ldots, x_{L-1})$

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- Challenging to find an efficient hardware solution
  - Large operand sizes x; small q_i

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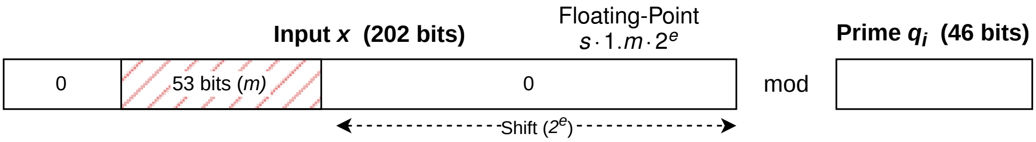

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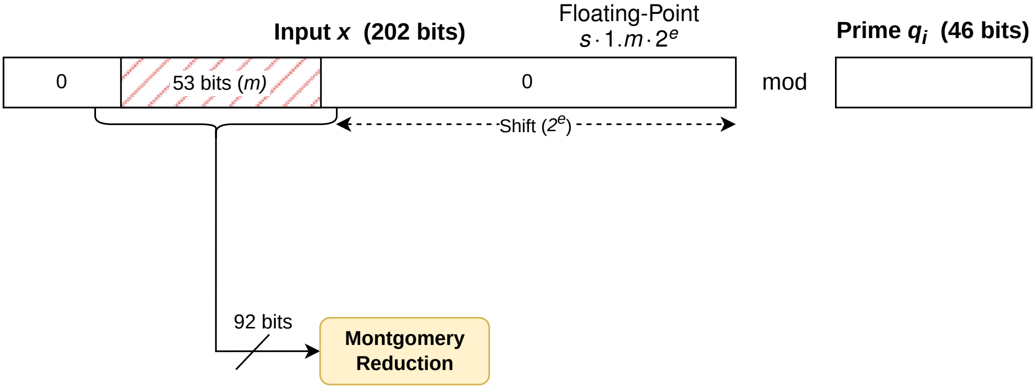

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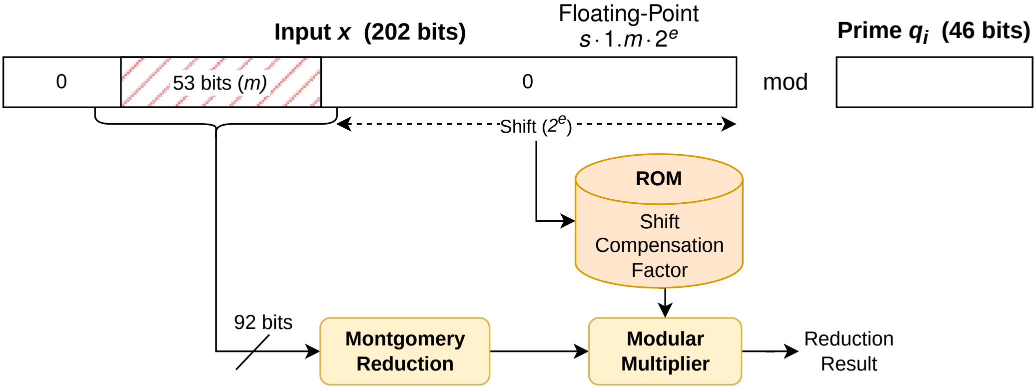

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  - Kintex-7 FPGA on Genesys2 board
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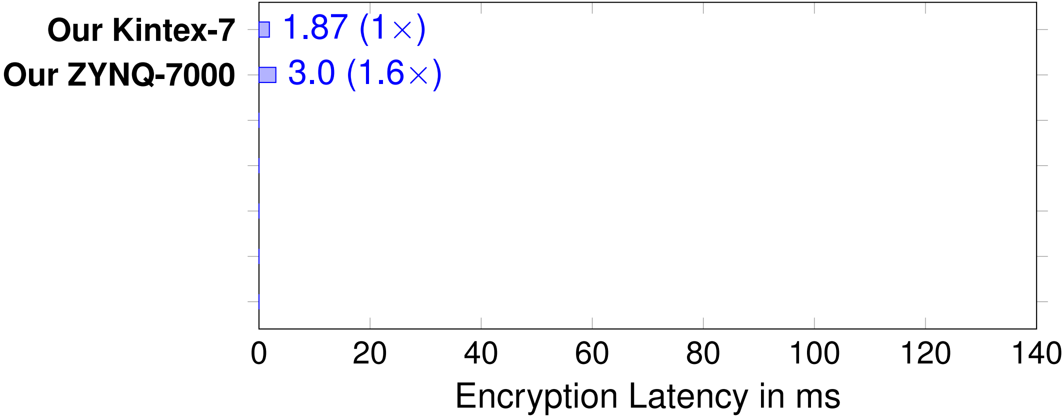

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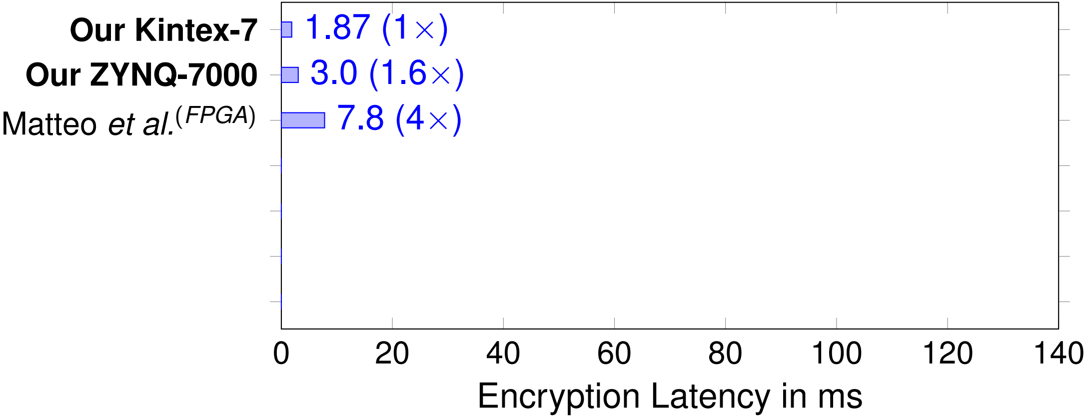

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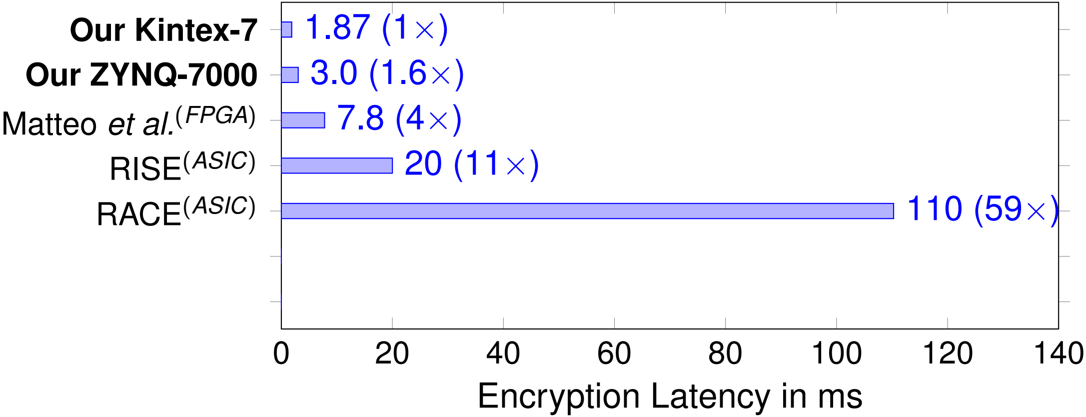

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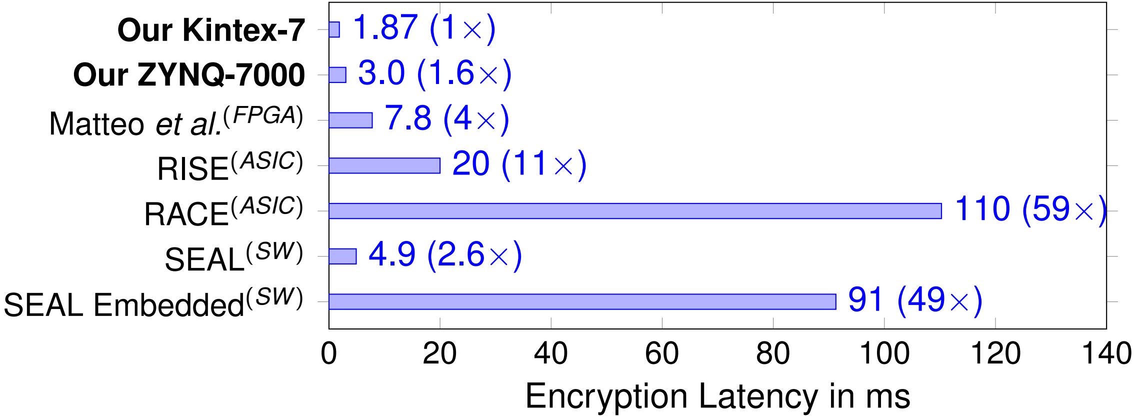
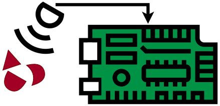


Performance Figures: Encryption

Our accelerator (FPGA)	**Intel Core CPU**	**Improvement**
200 MHz	2.3 GHz	11.5× lower
534 Enc/s	204 Enc/s	2.6×
5.8 mJ/Enc	73.5 mJ/Enc	12.7×



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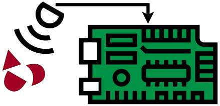

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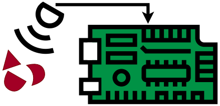
200 MHz	2.3 GHz	11.5× lower
534 Enc/s	204 Enc/s	2.6×
5.8 mJ/Enc	73.5 mJ/Enc	12.7×



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- First hardware accelerator covering all client operations in CKKS
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- Novel hardware-friendly approach for RNS
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Aloha-HE

A Low-Area Hardware Accelerator for Client-Side Operations in Homomorphic Encryption

Florian Krieger, Florian Hirner, Ahmet Can Mert, Sujoy Sinha Roy
Institute of Applied Information Processing and Communications, TU Graz

January 31, 2024

References

CKKS Scheme: J. H. Cheon, A. Kim, M. Kim, and Y. Song, “Homomorphic encryption for arithmetic of approximate numbers,” in Advances in Cryptology – ASIACRYPT 2017, T. Takagi and T. Peyrin, Eds. Cham: Springer International Publishing, 2017, pp. 409–437.

Microsoft SEAL: “Microsoft SEAL (release 4.1),” https://github.com/Microsoft/SEAL, Jan 2023, microsoft Research, Redmond, WA.

SEAL-Embedded: D. Natarajan and W. Dai, “Seal-embedded: A homomorphic encryption library for the internet of things,” IACR Trans. on Cryptographic Hardware and Embedded Systems, vol. 2021, no. 3, p. 756–779, Jul. 2021.

RACE: Z. Azad et al., “Race: Risc-v soc for en/decryption acceleration on the edge for homomorphic computation,” in Proceedings of the ACM/IEEE International Symposium on Low Power Electronics and Design. Association for Computing Machinery, 2022.

RISE: Z. Azad et al., “Rise: Risc-v soc for en/decryption acceleration on the edge for homomorphic encryption,” IEEE Transactions on Very Large Scale Integration (VLSI) Systems, pp. 1–14, 2023.

Matteo *et al.*: S. D. Matteo, M. L. Gerfo, and S. Saponara, “Vlsi design and fpga implementation of an ntt hardware accelerator for homomorphic seal-embedded library,” IEEE Access, vol. 11, 2023